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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/360,025	07/23/1999	SHINKEN OKAMOTO	2418.05-US-0	3581

7590 02/09/2005

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EXAMINER	
LAMARRE, GUY J	

ART UNIT	PAPER NUMBER
2133	

DATE MAILED: 02/09/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/360,025	OKAMOTO, SHINKEN	
	Examiner	Art Unit	
	Guy J. Lamarre, P.E.	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 October 2004* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *13,14,16,17 and 25-40* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *13,14,16,17 and 25-40* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *23 July 1999* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

FINAL OFFICE ACTION

0.1 This office action is in response to Applicants' amendment of *05 October 2004*.

0.2 Claims 13-14, 16-17, 25-33 are amended; Claims 34-40 are added. Claims 13-14, 16-17 and 25-40 remain pending.

0.3 The prior art rejection of record are withdrawn in response to Applicants' amendment.

Response to Arguments

0.4 Applicants' arguments have been fully considered and are deemed persuasive only to the extent that operation status is not mentioned per se, and newly ECC limitations were not addressed in previous the office action.

However, memory operation status monitoring comprises monitoring memory transfer operations, such as write/rewrite operations. Thus such operation status limitation does not depart from the teachings of the prior art of record e.g., in **Yamagami**'s Fig. 18.

The prior art of record discloses ECC means, e.g., in **Yamagami**'s Fig. 21.

Yamagami and **Yoshito** are analogous arts because IC memory design is taught.

Claim Rejections - 35 USC ' 103

1. **Claims** 13-14, 16-17 and 25-40 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Yamagami et al.** (US Patent No. 6,130,837; 25 November 1992) in view of **Yoshito et al.** (JP Publication No. 62290989; 17 December 1987) in further view of **Snavely** (US Patent No. 6,112,984).

As per Claims 13, 16, 25-40, Yamagami et al. substantially discloses, in Figs. 2 and 10, the procedure for the claimed memory unit comprising: a memory having a main memory area (block 21) and a spare memory area or write buffer (block 29), wherein said main memory area includes a plurality of data storage registers and wherein each of said data storage registers has an address, and wherein said spare memory area has a storage capacity; a display or status table (block 28); and a processor (block 23), wherein said processor transfers data stored in each of said addresses of said main memory area to said spare memory area upon a number of write

operations performed to a respective one of said addresses in said main memory reaching a predetermined value (or frequency of error Fig. 2)), and wherein said processor drives said display or status table to indicate or display storage capacity status or condition or operation status. {See **Yamagami et al.,** Figs. 2 ,10, 13, 20, 23, and related description, in passim, wherein apparatus and method (including error frequency means in Fig. 2 and associated description in col. 4 line 61 et seq., Fig. 13 depicts ECC means whereby detected defective memory areas are flagged to subsequently be replaced, Figs. 14, 20, 23 depict monitoring means via status table, write operations tracking, flash memory) are described.}

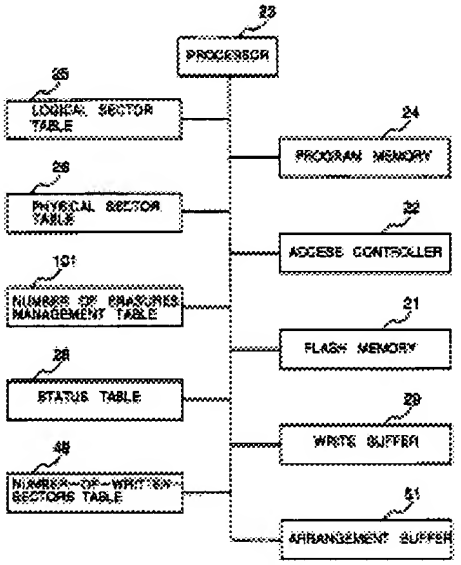


FIG.20

Not specifically described in detail in **Yamagami et al.** is the step whereby memory indicating means is via a **display means for displaying** remaining amount of said storage capacity in said spare memory upon a remaining amount of said storage capacity reaching a predetermined remaining capacity. **However** such approach is well known. For example, **Yoshito et al.,** in an analogous art, discloses a "Memory Card," wherein such techniques are described. {See **Yoshito et al.,** Id., ABSTRACT.} **Therefore**, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify the procedure of **Yamagami et al.** by including therein a **display means** as taught by **Yoshito et al.,**

because such modification would provide the procedure disclosed in **Yamagami et al.** with a technique whereby "***storage capacity of a memory is visually provided via a display terminal.***" {See **Yoshito et al.,** ABSTRACT.}

Not specifically described in detail in **Yamagami/Yoshito et al.** is the step whereby operation status is displayed is via a **display means**. **However** such approach is well known. For example, **Snavely,** in an analogous art, discloses a *ROM 121* or flash memory the operation status thereof is displayed on a liquid crystal display *LCD 91*. **Therefore**, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify the procedure of **Yamagami/Yoshito** by including therein operation status **display means** as taught by **Snavely**, because such modification would provide the procedure disclosed in **Yamagami/Yoshito** with a technique whereby a system operator can monitor ***storage capacity of a memory visually via a display terminal.***

As per Claims 14, 17, Yamagami et al. substantially discloses, in col. 13 line 13 et seq., the procedure for the claimed memory unit as in claim 13, wherein said processor compares said remaining amount of said storage capacity with a plurality of different values of said predetermined remaining capacity, wherein the comparison produces a plurality of different results, and wherein said processor drives said display or external unit in different manners dependent upon said plurality of different results.

As per Claim 18, Yamagami et al. substantially discloses, in Fig. 4 and col. 6 line 2 et seq., the procedure for the claimed memory unit as in claim 13, wherein said processor drives the display upon said number of write operations or error frequency (col. 4 line 61 et seq.) performed to a respective one of said addresses in said main memory reaching a predetermined number or frequency (col. 4 line 61 et seq.).

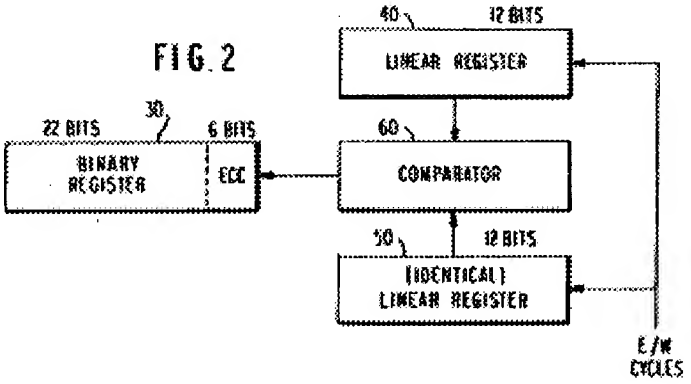
Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless -
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3.1 Claims 13-14, 16-17 and 25-40 are rejected under 35 U.S.C. 102(b) as being anticipated by **Pricer (US Patent No.** 5222109; June 22, 1993**).**

As per Claims 13-14, 16-17 and 25-40, Pricer discloses the claimed procedure for displaying/indicating non-volatile/flash memory operating status and error detection/correction means, and data transfer/write/rewrite counting means, e.g., Figs. 2-4,



'A nonvolatile storage system including several data storage arrays; a counter storage array for storing values indicating the remaining useful life of each of the data storage arrays; and a device for controlling access to each of the data storage arrays as a function of the values stored in each counter array. The counter array has an appreciably longer useful life than any of the data storage arrays'.... the nonvolatile memory blocks are tested by subjecting the memory blocks to relatively short erase/write cycles to determine which memory blocks are likely to fail first, and which memory blocks have a better than average endurance to erase/write cycles. Those memory blocks which are likely to fail first could be loaded with a pre-count so that if these blocks are subjected to substantially more than average usage, the blocks would be reallocated early, i.e., earlier than if the counter was not loaded with a pre-count. On the other hand, those memory blocks determined to have a better than average endurance to erase/write cycles could be used as substitutional blocks. These high endurance memory blocks would

later be substituted for high usage addresses. Thus, the strongest storage cells would subsequently be used for the highest usage addresses. Further, the counters of the system could be combined with a redundancy bad-block scheme wherein those memory blocks determined to have extremely poor endurance to erase/write cycles are preloaded with a full count.'

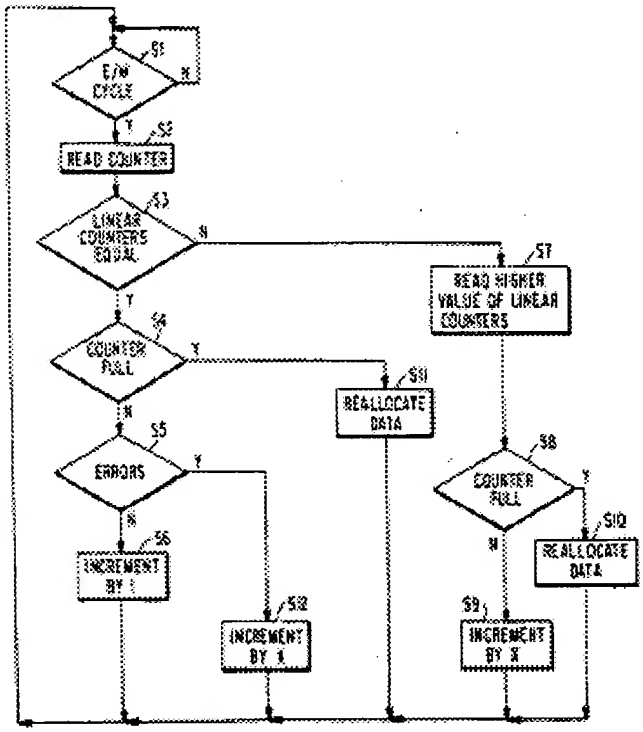


FIG. 4

Conclusion

4. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL.** See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

4.1 Any response to this action should be mailed to:

Commissioner of Patents and Trademarks, Washington, D.C. 20231

or faxed to: (703) 872-9306 for all formal communications.

Hand-delivered responses should be brought to Customer Services, 220 20th Street S., Crystal Plaza II, Lobby, Room 1B03, Arlington, VA 22202.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Guy J. Lamarre, P.E., whose telephone number is (571) 272-3826. The examiner can normally be reached on Monday to Friday from 9:30 AM to 6:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert De Cady, can be reached at (571) 272-3819.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (571) 272-3609.

Information regarding the status of an application may also be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Guy J. Lamarre, P.E
Primary Examiner
2/7/05